AMENDMENTS TO THE SPECIFICATION

Replace the paragraphs on page 1, lines 11-16, with the following:

METHOD AND APPARATUS FOR TIME-SLICED AND MULTI-THREADED DATA PROCESSING IN A COMMUNICATION SYSTEM

Ser. No. ~~To Be Assigned~~09/920,093, ~~Attorney Docket Number 9824-045-999~~filed July 31, 2001

DYNAMICALLY RECONFIGURABLE UNIVERSAL TRANSMITTER SYSTEM

Ser. No. ~~To Be Assigned~~09/922,484, ~~Attorney Docket Number 9824-070-99~~filed August 3, 2001

Replace the paragraph beginning on page 10, line 7, with the following:

Hardware resources 102b, 106b, 110b, and 111b are applied to a single computation process within a given system cycle in one embodiment. However, in another embodiment, hardware resources 102b, 106b, 110b, and 111b can be enhanced by running them at a clock rate higher than that required by a process in a given system cycle. That is, the hardware resources can be operated at a frequency that is higher than the data rate for a communication protocol implemented on communication device 100a. In this manner, resources of individual computation components, a receiver processor, can be time-shared across multiple computation processes, e.g., several multipaths and/or multiple channels. Additional information on the design and implementation of configurations into a configurable communication device is provided in co-pending U.S. patent application Ser. No. 09/492,634 entitled "IMPROVED APPARATUS AND METHOD FOR MULTI-THREADED SIGNAL PROCESSING" by Subramanian et al., ~~attorney docket number MORP-P002~~filed January 27, 2000. This related application is commonly assigned, and is hereby incorporated by reference. More detail on time-sharing of hardware resources is described in FIG. 1C. By using the software-based allocation and scheduling of hardware resources, communication device 100a benefits from flexible and dynamic use of hardware resources that saves power, improves performance, allows changes of controlling algorithms, and provides extended lifespan of the device.

Replace the paragraph beginning on page 11, line 28, with the following:

Tracking scheduler 102a is also referred to as an allocator, as described in co-pending U.S. patent application Ser. No. 09/772,584 entitled "A Wireless Spread Spectrum Communication Platform Using Dynamically Reconfigurable Logic", by Subramanian et al., ~~attorney docket number 9824-0061-999~~filed January 29, 2001. Additional information on the design and implementation of configurations into a configurable communication device is provided. This related application is commonly assigned, and is hereby incorporated by reference.

Replace the paragraph beginning on page 12, line 1, with the following:

Elements 156a through 156n of hardware resource 102b include a conventional ASIC portion 157 coupled to a programmable and distributed micro digital signal processing units (micro DSP) 159 in the present embodiment. Both types of devices are coupled together to perform a desired function. The uDSP can perform repetitive functions, e.g., math operations, useful for a given application while the ASIC performs more function specific tasks for finger element 156a. Additional information on the content and function of a uDSP is provided in co-pending U.S. patent application Ser. No. ~~_____~~09/912,721 entitled "Distributed Micro Instruction Set Processor Architecture for High-Efficiency Signal Processing" by Chen et al., ~~attorney docket number 9824-0067-999~~filed July 24, 2001. This related application is commonly assigned, and is hereby incorporated by reference. In another embodiment, elements of hardware resources 102b can be either all ASIC or all uDSP or any combination thereof.

Replace the paragraph beginning on page 12, line 13, with the following:

In another embodiment, hardware resources 102B, e.g., finger elements 156a through 156n, are limited to performing a single communication protocol, while in another embodiment; hardware resources are configurable to perform any one of a wide range of communication protocols. For example, co-pending U.S. patent application Ser. No. 09/751,783, entitled "A Configurable All-Digital Coherent Demodulator System for Spread Spectrum", by Ravi Subramanian, ~~attorney docket number 9824-0037-999~~filed December 29, 2000, is configurable to accommodate a wide range of

communication protocols. This related application is commonly assigned, and is hereby incorporated by reference.

Replace the paragraph beginning on page 13, line 27, with the following:

By reusing hardware, a given system can be tailored to individual needs by scaling the clock rate and thereby the virtual resources created by the multiple processing cycles with a given system cycle. M can be any value for a given application. The greater the number of virtual resources required, the higher a clock rate for the resource can be scaled. Also, the greater the number of virtual resources, the greater the amount of memory required to store context data save from one virtual use, and used to setup the virtual use for the next system cycle. Because each virtual use of a given hardware element is completed within a given system cycle, they appear to be performed in parallel as concurrent operations, though only a single hardware resource is used. More information on time-sharing of hardware resources is described in co-pending U.S. patent application Ser. No. ~~_____~~09/920,093 entitled "METHOD AND APPARATUS FOR TIME-SLICED AND MULTI-THREADED DATA PROCESSING IN A COMMUNICATION SYSTEM," by Rieken et al., ~~attorney docket number 9824-045-999~~filed July 31, 2001. This related application is commonly assigned, and is hereby incorporated by reference. Additional information is also provided in co-pending U.S. patent application Ser. No. 09/492,634 entitled "IMPROVED APPARATUS AND METHOD FOR MULTI-THREADED SIGNAL PROCESSING" by Subramanian et al., ~~attorney docket number MORP-P002~~filed January 27, 2000, now abandoned. This related application is commonly assigned, and is hereby incorporated by reference.

Replace the paragraph beginning on page 21, line 8, with the following:

Referring now to FIG. 3D is a table of computer memory fields that track users of software-based allocation and scheduling of hardware resources, in accordance with one embodiment of the present invention. Primary table 380A lists groups of hardware resources by a group identification in column 381 and by a pointer to a secondary table that identifies the start location for the control information on the hardware resources slated for the group. Primary table can provide a reference back to an ID table, e.g., table 350. The last entry in primary table is for B, after which the fist line

in primary table is resume, e.g., pointer end traverses to the first line of the table. Secondary table includes an on/off column to turn control parameters for a hardware resource either on or off. No link list is listed in column 389 for all the entries in a group, e.g., first block A 370. This is because each entry has a default pointer to the next line in the table. In this manner, total flexibility throughout the table is eliminated at the benefit of ease of implementation and speed through which the table may be traversed. However, a link address can be implemented for any line of a hardware resource. This list can be referred to as a chunk list in that all the hardware elements in first block A 370 are implemented in a sequential fashion as the default address link sequence. While the present embodiment provides a specific quantity of table and columns in each table, the present invention is well suited to utilizing more or less columns with different types of information for other purposes. The flexibility and implementation ease of the present invention is still maintained with these alternative embodiments. Additional information on the design and implementation of primary and secondary tables 308A and 380B respectively, is provided in co-pending U.S. patent application Ser. No. ~~_____~~09/922,484 entitled "DYNAMICALLY RECONFIGURABLE UNIVERSAL TRANSMITTER SYSTEM" by Medlock et al., ~~attorney docket number 9824-070-999~~filed August 3, 2001. This related application is commonly assigned, and is hereby incorporated by reference.

AMENDMENTS TO THE TITLE

Please change the title to: METHOD AND APPARATUS FOR SOFTWARE-BASED ALLOCATION AND SCHEDULING OF HARDWARE RESOURCES IN A WIRELESS COMMUNICATION DEVICE